

Radiation Evaluation Method of Commercial Off-the-Shelf (COTS) Electronic Printed Circuit Boards (PCBs)

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Abstract:

We present a radiation evaluation methodology and proton ground test results for candidate COTS PCBs and their associated electronics for low-altitude, low-inclination orbits. We will also discuss the implications associated with mission orbit and duration.

I. INTRODUCTION

Workstation class processor architectures and high-performance space subsystems using commercial hardware have an enormous potential for enabling scientific mission capabilities while drastically reducing developmental and life cycle costs [1]. The performance, cost, and schedule benefits gained from using commercial electronics in space applications are as readily apparent as the perceived difficulties in incorporating them into the hardware. However, with experience gained from the commercial satellite sector and parts assurance studies underway at a variety of institutions, the trend toward off-the-shelf hardware is increasing. In this paper, we will present an extension of previous discussions and data sets [2]. The following areas will be examined:

- Challenges involved with radiation evaluation of COTS PCBs;
- A proposed evaluation philosophy extending the method stated in ref. [3] with two examples:
 - Application of this method to the NASA SPARTAN 251 program including ground irradiation test results; and
 - Initial COTS hardware evaluations for the International Space Station (ISS) Fluids and Combustion Facility (FCF), and
- A discussion of the limitations and recommendations for the use of the proposed philosophy. In particular, the orbit and mission duration parameters will be addressed.

II. CHALLENGES OF USING COTS PCBs

COTS hardware provides unique challenges to the space program intent on their usage. This is true for more than

radiation issues. One such approach has been presented discussing the non-radiation (and briefly, a few of the radiation) issues such as thermal, mechanical, and vacuum performance [4].

Some of the radiation challenges include:

- The inability to trace die heritage which leads to uncertainties in applying results of one test PCB to another,
- The issue of piecepart versus board level tests where board performance, not device performance is being monitored limiting the precision of knowledge on sensitive devices and/or nodes within a device,
- The possibility of “board-to-board” IC variances (different manufacturers, lots, etc.) for “copies” of the “same” PCBs with the “same” bill-of-materials (BOMs),
- The ability to simulate the space radiation environment with a single particle test (note: this issue is not limited to COTS PCBs, but to all radiation tests),
- The limited testability of PCBs due to complex circuitry (limited insight on how the internal device performance and ability to monitor that performance) and packaging issues such as penetration of a heavy ion to the sensitive volume in a flip-chip or plastic encapsulated microcircuit (PEM) (again not limited to COTS PCBs, but exacerbated by them) or testing of dual-sided PCBs or other circumstances where the radiation beam is impinging on multiple components (this also affects dosimetry as to radiation exposure levels), and
- Limited test statistics due to practical matters such as number of test samples (limited due to cost of hardware), facility beam usage (cost of facility), and complexity of detailed test fixtures and test systems (non-recurring engineering or NRE costs).

III. EVALUATION PHILOSOPHY

In this section, we will discuss the proposed evaluation philosophy extending [3] for use with COTS boards for

missions of limited duration. The method proposed in [3] is synopsised as follows:

- Define the hazard
- Evaluate the hazard
- Define requirements
- Evaluate device usage
 - Screen parts lists
 - Radiation test devices with no existing data or perform radiation lot acceptance tests (RLATs)
 - Performance predictions (e.g., Single Event Effect or SEE rates)
- “Engineer” with designers
 - Alternate device selection,
 - Mitigation options,
 - System validation, ...
- Repeat above as necessary

The philosophy embodied here is to treat a PCB as a device, i.e. determine system performance as opposed to simply device performance. This is not a new concept. However, COTS boards exaggerate this issue due to the large unknowns such as:

- Limited information available on BOMs/parts list (no vendors, lot date codes, etc.),
- Lot-to-lot variability, as well as
- The other challenges delineated earlier.

The main areas of difference from the established method are in the step entitled “Evaluate device usage” while additionally exaggerating the importance of system-level mitigation solutions. The first change is in reviewing a COTS-board parts list. Typically, multiple board copies are purchased. It is assumed that all boards have “same” components. This is not necessarily a true statement. The following illustrates, briefly, the steps involved.

- Parts list review:
 - Identify devices with unknown characteristics
 - Gather data on devices of device families with existing data
- Identify “critical” systems and devices
 - This is a system engineering function whereby it is determined which radiation-induced degradation may impact system functionality
- Recommend radiation testing as “confidence gathering” for critical devices/board

This last step is the true variance from [3]: instead of performing RHA or RLATs on piecpart devices, for COTS PCBs, we are providing a confidence gathering process to increase the likelihood of mission success. That is, the test performed provides some level of hope (not statistical

confidence as one would gain by testing samples of a flight lot of devices) that the flight PCB may act similarly to the test article. We will discuss further two actual test philosophies: one for a short duration mission (SPARTAN 251), and one for a longer duration mission (ISS FCF).

IV. SPARTAN 251 OVERVIEW AND PCBs OF INTEREST

SPARTAN 251 is a NASA mission aimed at low-Earth (LEO), low inclination orbits such as the Space Shuttle. It is a short duration mission with a planned lifetime of less than thirty days. In this type of low inclination LEO, the main hazard to electronic systems from radiation is the trapped protons that occur in the South Atlantic Anomaly (SAA). Due to the short mission duration and orbit, total ionizing dose (TID) and displacement damage (DD) effects are not of concern, heavy ions are a very small concern (low numbers of particles, short timeframe = low probability of an event), and proton-induced SEEs are the prime issue.

The Central Unit Electronics (CUE) box is a controller and data gathering interface for portions of the SPARTAN 251. Its basic functions include processing, serial interfaces, memory, MIL-STD-1553 interfaces, and a custom uplink/downlink interface to the ground. The box is based on the commercial standard Compact Peripheral Component Interconnect (CPCI) bus and it’s associated commercially available carriers and chassis’. A block diagram of the CUE box is seen in Figure 1.

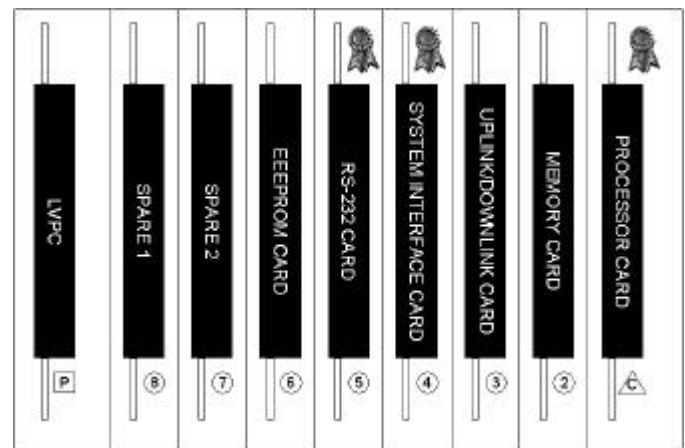


Figure 1: Central Unit Electronics (CUE)

Table 1 lists the candidate PCBs for radiation tests with a device list (or device under test (DUT) list) either from BOMs, visual inspection, or in some cases, both since the BOMs were inconsistent with visual inspection. Figure 2 is a picture of one of the candidate boards from Ziatech. Based on our experiences with COTS-style devices, the larger ICs that have a high pin-count tend to be of most concern for radiation sensitivity (highest gate counts and circuit complexity).

Table 1.
SPARTAN 251 PCBs and DUTs

Manufacturer	Mfr. Part Number	DUTs	Board Description	Test Date	Test Facility
Greenspring	CPCI-100	Unknown	Dual IP 3U Carrier	Sep-97	IUCF
Greenspring	Unknown	IPUS, PLX9060, Zilog, Altera	IP Universal Serial Interface Module	Sep-97	IUCF
Greenspring	IP 1553	DDC 1553 Components	MIL-STD-1553 Interface	Sep-97	IUCF
Greenspring	CPCI-200	Altera EPM128, PLX9060, Harris 74HCT123, Harris 74AC74, IDT 74FCT162952, IDT 49FCT805, IDT FCT244, IDT 74FCT16244, NSC LM339, XXX74AC04, XXX74AC08, XXX76AH93546, SM1100JY OSC, Dallas DS1233	6U IP Carrier	May-98 & Jun-98	UCD CNL & IUCF
Greenspring	Unknown	XC3042 FPGA, XL93CS46, Diodes, XC1765 Serial PROM, LTC1257, LM339A, LM324, SP485	HV-Unidig Driver	Jun-98	IUCF
Greenspring	Unknown	Zilog AM8530, MC1488, SN75172, SN75173, 27LS19, Xtal	IP Serial Driver	Jun-98	IUCF
Greenspring	Unknown	68230, 27LS19, PALC16R6, LM337HV, Q17, ILQ2, IRFD9020	IP Optocoupler Driver	Jun-98	IUCF
Ziatech	ZT-6500	Intel P166, Custom 1449 ASIC, Samsung DRAM, Intel 28F010 Flash, Intel 28F032 Flash, PCI Master ALI, PAL, IMI SC478, MAX 767, LV16245	CPCI Pentium Processor	Sep-97	IUCF
Alphi	Unknown	ABRACON 32MHz Osc., AMCC PCI S5933, AMD Mach445, AT24C04, Dallas DS1232, IDT74FCT244, IDT74FCT374, IDT74FCT521, IDT74FCT543, IDT74FCT16245, IDT74FCT16374, Harris CD74ACT08, Harris CD74ACT139, Harris CD74HCT123, Harris CD74HCT00, SUPETRTREX VN0104N3, SUPETRTREX VN0104N7	3U IP Carrier	May-98 & Jun-98	UCD CNL & IUCF
Alphi	SCC-04	Microchip 28C16A, Lattice GAL26CV12B, ZILOG Z8523010, TI SN75174, TI SN75175, Motorola 74AC04, Epson SG-615P (Osc)	IP Serial Driver	Jun-98	IUCF
Force	CPCI-3603	LIN 7702, LIN 7705, X24C04, 74F08, 74ABT125, 74ABT373, 74ACT14, 74LVT245, COM 82371, AM28F020, DRAM, Intel E28F008SA, LIN LTC1266, L4478, LATTICE 2032-135L, LATTICE 1016-125LT, MBRS130LT3, MAX734, MPC970, OSC, COM TL16C550C, S16426DQ, X8853606, XPC106, XPC603	CPCI PowerPC Processor	May-98 & Jun-98	UCD CNL & IUCF
Plessey	Unknown	Plessey 2021 - Correlator	GPS Correlator/Front-end	Sep-98	UCD CNL
Cogent Computers Inc	CMA-401A	DEC SA110 STRONGARM, MACH466 CPLD, ST16C2552 UART	STRONGARM Processor	Sep-98	UCD CNL



Figure 2: Ziatech ZT-6500 3U Compact PCI Pentium Board.

V. SPARTAN 251 TEST PROGRAM

Assuming that multiple copies of each PCB are being procured, two types of proton irradiations for SEE: a high fluence test on one PCB followed by low fluence testing on actual flight hardware. The testing on the CUE hardware followed the below general procedure:

- Define a “martyr” board (i.e., high fluence level) for proton SEE irradiation.
- Irradiate this board to a proton fluence N times greater than predicted mission fluence (mapping a multi-energy spectrum into a monoenergetic test) monitoring SEE and limited TID/DD performance. For CUE, this level of exposure simulates an environment over ten times harsher than predicted for a thirty day shuttle orbit.
- Perform proton irradiations on PCBs
 - Tests were performed at Indiana University Cyclotron Facility (IUCF) and University of California at Davis Crocker Nuclear Laboratory

(UCD CNL). Prime beam energy incident on the DUTs at these facilities were 195 and 63.3 MeV, respectively. Dosimetry at both facilities is within fifteen percent (thus, results presented later have a similar spread).

- Irradiate in steps, while attempting to isolate individual ICs during irradiations in order to determine sensitive components
 - This is difficult due to beam spread, double-sided PCBs and their associated backside irradiation issues, tight PCB layouts, etc.
 - Steps were typically on the order of 100–500 rads(Si). This step irradiation method, minimizes the probability of test failure from TID/DD concerns prior to gathering significant SEE information.
- If the martyr PCB passes (as defined by the systems engineer), then
- Irradiate flight hardware boards to a low-level (“non-destructive”) of proton fluence (i.e., 100 rads (Si)) in the hope that the flight board behaves in a similar manner to the martyr.
- No heavy ion SEE tests were performed.

The martyr board is used for three reasons. These are:

- To pre-screen whether to irradiate flight hardware or not based on SELs, TID failure, etc.,
- To gain limited TID and displacement damage knowledge, and
- To gain confidence for flight SEU performance. For example, assuming a test fluence of ten times mission predicted levels and similarity between martyr and flight hardware, if no “events” were noted during martyr test, then the flight hardware has only a 1 in 10 chance of having an event during mission lifetime.

VI. ISSUES WITH THE SPARTAN CUE RADIATION TEST METHOD

There are many issues with this method varying from reliability to test environment to handling concerns. First, proton testing provides key information on SEE, TID, and DD, but does not adequately cover heavy ion-induced SEE. Albeit for this mission heavy ion-induced destructive conditions are a small concern, it is still a non-zero possibility. It should be mentioned that heavy ion testing on this type of hardware is difficult and expensive at best due to facility limitations (penetration range of ions, availability of ions, or cost for facility) and packaging issues.

Second, the low fluence test on flight hardware is “non-destructive”. Several concerns exist over this statement. Some particle fluence/dose has been placed on flight hardware pre-flight. Without full knowledge of the TID/DD characteristics,

this is risky though one assumes that a few hundred rads (Si) should not have gross effects on device performance or lifetime. In addition, the handling of flight hardware at test sites is vastly less controlled than in a clean room or typical flight hardware laboratory constraints. Lastly, the board has been stressed electrically during test conditions. Reliability effects from this are unknown, but suspect.

The third issue is comparing the results between the martyr board and the flight hardware. If the results appear similar, this does not imply that an anomaly not observed during martyr board irradiation will not occur on the flight board during its mission life. It may simply imply that a lower or low [5] probability event that might have occurred if testing had continued to an even higher fluence on the martyr board or from a difference in components such as lot-to-lot variance between the two “copies”. If the results are different between the two copies, it may be due to variance in components or a small probability event [5]. In any case, without full traceability of components on the PCBs, it is impossible to “guarantee” assurance.

Test isolation provides the fourth challenge. Because we are typically monitoring system-level performance and not device performance, it is difficult to determine the exact cause of events that occur during testing. Picture, for example, a stack of memory devices. Unless has sufficiently detailed information such as physical versus logical bit addressing, we can say that an error occurred, but not where. This same principle applies to this type of proton SEE test where multiple components are often in the beam at one time. A complex and smart suite of test hardware and software is required to provide, at best, limited information.

One faces the issue of application-specific sensitivities versus generic test results. Radiation testing is typically performed prior to the completion of the actual flight application coding. What this implies is that since single event upsets (SEUs) are often dependent on operating frequency, duty cycle, and sensitive time windows, the test suite which may utilize different utilization factors in hardware, etc. may or may not provide insight into the actual PCB sensitivity. This issue is true for more than PCBs.

Lastly, with such a small sample size (one significant data point and another weak point), the statistics on the results are poor.

What is gained by this kind of test procedure is some limited confidence that the flight PCBs may act like the martyr board as well as a pre-screen for obvious problems. For short duration missions (days to weeks) in a relatively benign orbit, this is a reasonable approach. For longer mission duration or harsher environmental concerns, this method may prove to be too high a risk to mission success.

VII. SPARTAN 251 PROTON IRRADIATION RESULTS

In all, thirteen board types were irradiated. The cumulative fluence levels on the martyr boards were between 3.5 and 5.0×10^{11} protons/cm². The flight hardware was tested to levels of $\sim 1 \times 10^7$ protons/cm². Limiting cross-sections for lack of observed events should be based on these fluence levels.

Multiple types of errors and parameters were monitored. These include: data errors, control errors that required a soft reset (reset pulse of software reload), control errors that required a power cycle, destructive conditions, PCB functionality, and limited parametrics. All of these types of conditions were noted at some point during the COTS PCBs irradiations.

Table 2 provides a synopsis of the test results for a variety of candidate PCBs. This includes noting the suspected sensitive device(s), the type of error noted, and rough (with admitted poor statistics) cross-sectional information on the condition results.

Several results are of key interest. As expected, devices with higher pin counts proved to be the most sensitive to SEE. This includes observances of an SEL on an ASIC and on a FPLD device as well as multiple soft errors on commercial microprocessors, peripherals, DRAMs, and other ASIC or programmable devices. In addition, one PCB failed functionally at a dose of just a few krad (Si). This was on an optocoupler driver card. Damage on optocouplers has been a key issue to the aerospace community in the past several years, so we might have expected this result if sufficient detail was available on that card's components [6].

One further result is of note, one board type provided differing results between the martyr and flight hardware. Again, it is difficult to determine what caused this (part variance, design change, etc.), simply that the result was repeatable (i.e., not a one time event).

For SPARTAN 251, hardware selections were made for flight based on this gathered data. However, design changes (architectural watchdogs and software techniques) were incorporate based on these results.

Table 2.
SPARTAN 251 Radiation Test Results

Manufacturer	Mfr. Part Number	Board Description	Brief Results	Suspected sensitive device or prime DUT	Data Errors	Control Errors	SEL	Notes
Ziatech	ZT-6500	CPCI Pentium Processor	SEU, SEL observed	Intel P166	none observed to test levels	1.2×10^{-8} cm ² /device	none observed to test levels	System halt: required reset
				1449 Custom ASIC	1.1×10^{-10} cm ² /device	3.3×10^{-11} cm ² /device	1.1×10^{-11} cm ² /device	Control errors required reset: SEL lcc>50mA
				Samsung DRAM	6.3×10^{-15} cm ² /bit	none observed to test levels	none observed to test levels	Single bit errors only
				ALI PCI Master	none observed to test levels	none observed to test levels	none observed to test levels	
				Intel Flash	none observed to test levels	none observed to test levels	none observed to test levels	
Greenspring	CPCI-100	Dual IP 3U Carrier	No events		none observed to test levels	none observed to test levels	none observed to test levels	
Greenspring	IP 1553	MIL-STD-1553 Interface	No events		none observed to test levels	none observed to test levels	none observed to test levels	
Greenspring	Unknown	IP Serial Driver	SEL	Altera FPLD	none observed to test levels	none observed to test levels	3.8×10^{-11} cm ² /device	SEL lcc>3mA: destructive
Alphi	Unknown	3U IP Carrier	No events		none observed to test levels	none observed to test levels	none observed to test levels	
Greenspring	CPCI-200	6U IP Carrier	No events		none observed to test levels	none observed to test levels	none observed to test levels	
Force	CPCI-3603	CPCI PowerPC Processor	SEU	XPC603 processor or X24C04 PROM	1×10^{-10} cm ² /dev	2.06×10^{-9} cm ² /device	none observed to test levels	Functional interrupts
				DRAM	6.5×10^{-8} cm ² /device	none observed to test levels	none observed to test levels	Multiple DRAMs in beam: all single bit errors
				DRAM	1.1×10^{-10} cm ² /device	none observed to test levels	none observed to test levels	Multiple bit error observed on low fluence test but not on martyr
				Lattice CPLD or 52371 or MPC970	7.8×10^{-11} cm ² /device	1.2×10^{-10} cm ² /device	none observed to test levels	
Greenspring	Unknown	IP Optocoupler Driver	SEU, Displacement damage on optocoupler	ILQ2 optocoupler	$< 5 \times 10^{-12}$ cm ² /dev	none observed to test levels	none observed to test levels	Functional failure due to displacement damage on ILQ2 at 1.6×10^{-10} 195MeV protons/cm ²
Greenspring	Unknown	HV-Unidig Driver	SEU	XC3042 FPGA	none observed to test levels	1×10^{-11} cm ² /device	none observed to test levels	Event triggered a processor error on the control card
Greenspring	Unknown	IP Serial Driver	SEU	Zilog AM530	none observed to test levels	1×10^{-11} cm ² /device	none observed to test levels	Probable PCI bus halt requiring power reset
Actis	SCC-04	IP Serial Driver	SEU	GAL26CV12B or 28C16A	none observed to test levels	1.1×10^{-10} cm ² /device	none observed to test levels	Continuous fails of R/W and lcc drop by 80 mA noted: cleared by reset pulse
Plessey	Unknown	GPS Correlator/Front-end	SEU	Plessey 2021	NA	see note	none observed to test levels	Loss of lock observed during test, but setup was not able to capture. Functional interrupt also observed with cross-section $< 1 \times 10^{-11}$ cm ² /device. Cleared by power reset.
Cogent Computers Inc	CMA-401A	STRONGARM Processor	SEU	DEC SA110 or MACH468 CPLD	none observed to test levels	1.35×10^{-11} cm ² /device		Two types of events noted: one reset hardware automatically, other required a reset pulse

All results are for the martyr board unless otherwise noted
Test levels were to fluences of 3.5×10^{10} - 1.5×10^{11} protons/cm²

VIII. EVALUATING A LONGER DURATION MISSION

In this section, we will discuss the International Space Station (ISS) Fluid and Combustion Facility (FCF). We will present our analysis of their environment and discuss the review of the parts list obtained, as well as our recommendations for radiation tests.

The ISS FCF is a microgravity science payload currently being designed to conduct sustained, systematic fluid physics experiments within the manned bay of the ISS. Budget and schedule constraints, along with performance requirements have dictated a design approach centered around COTS boards. The FCF flight electronics are contained within 3 large racks with multiple modules and literally dozens of COTS (mostly Compact PCI) boards. As an indicator, the FCF power requirements are in excess of 1 kW, and almost all power will be consumed in COTS hardware.

The FCF is not mission-critical to the ISS, and some outages due to radiation effects can be tolerated. Destructive events would be problematic and excessively frequent disruptions due to recoverable SEEs would also be unwanted. We have attempted to apply the lessons learned from the SPARTAN test effort and apply them to the more challenging evaluation of the FCF hardware to form an initial assessment of the impact of the ISS radiation environment on the FCF hardware and associated science.

The ISS radiation environment concerning the FCF will be primarily energetic protons. The 500 km x 51.6 degree orbit is heavily geomagnetically shielded from cosmic rays except at the latitude excursions. Since the FCF will be located within the manned bay (with > 1000 mils Al equivalent shielding), it will be effectively shielded against electrons and low energy protons. Most protons will be encountered in the South Atlantic Anomaly (SAA). The annual fluence of protons will be 4×10^8 p/cm² over all energies, but due to the heavy shielding the average energy will approach 100 MeV.

Our experience with COTS boards is that only very limited indications of the components populating the boards are obtainable from the board vendors. Sometimes Bill of Material (BOM) listings are helpful, but more often the information provided is insufficient to identify the component with confidence. Our experience was that only around 10% of the components could be traced to test results on similar components, and the radiation response of most components are therefore largely unknown.

The planned test effort for FCF will use high energy protons (~195 MeV) to perform *in situ* board level tests of selected components at fluences approaching and exceeding the expected 10 year mission fluence of 4×10^9 /cm². The strategy relies on a set of test vectors to stimulate the various components in ways simulating flight software. By mounting the Board Under Test (BUT) on a remotely controlled positioning stage, incremental exposures of the Devices Under Test (DUTs) can occur in sequence. By exposing the

DUTs in a stepwise manner and monitoring for errors during each exposure, the sensitivity of each DUT can be assessed.

The key concern for FCF COTS boards is that protons may trigger destructive latchup in commercial CMOS devices. As a consequence, the boards selected for the first round of testing will be those heavily populated with large CMOS circuits. As a first cut metric, the pin count of a given device is useful in gauging its complexity. A PowerPC[®] based processor board will be evaluated in the first round of tests, and those results will determine the extent of subsequent testing. Evidence of latchup sensitivity, or excessively large soft error cross-sections may lead to consideration of alternate hardware choices or error mitigation strategies. These evaluations will include the risks already discussed regarding the lack of traceability of components on COTS boards. There will not be any attempt to expose flight hardware as in the SPARTAN project.

IX. DISCUSSION AND RECOMMENDATIONS

In this section, we will discuss the lessons learned and recommendations for flight programs. What is obvious is that one must take a system perspective when discussing the use of COTS boards; this becomes a risk management trade. One must know the radiation hazard (slight, severe, etc.) as well as the criticality of the system (mission critical to expendable) to determine whether COTS PCBs should even be considered. Once this has been determined, a test program may be entered. As a rule-of-thumb, low inclination LEOs most easily lend themselves to COTS board consideration, but even this has risks (heavy ion exposure, mission lifetime issues) as has been pointed out. The authors do not recommend consideration of COTS PCBs in more severe radiation environments such as polar orbits, geotransfer orbits, etc., unless a high risk is considered allowable. What is gained by these tests is a reasonable confidence for short duration low inclination LEOs and limited confidence for longer or harsher environment systems.

We view criticality from two perspectives:

- System criticality within a mission, and
- Board criticality within a system.

Due to the uncertainties and challenges previously discussed, we recommend use of COTS PCBs in non-critical mission applications, but not in critical applications. Then, depending on this system criticality, board-level proton tests are required on all critical boards within a system. As with the FCF, no irradiation of actual flight hardware is recommended, but only a copy of the flight hardware. Proton testing is also recommended (but not required) on hardware that is deemed of medium risk. One should also consider board-level heavy ion experiments or working with the PCB manufacturers to obtain piecepart samples for heavy ion device irradiations as a further means of reducing risk. Whenever feasible, the authors highly recommend piecepart irradiations be performed.

The SPARTAN 251 CUE testing provided several additional pieces of information with its martyr/flight board test procedure. First, it provided a sanity check: is there anything on the flight board we KNOW is an issue? If the flight board reacts in a similar manner to the martyr, there is some hope that it may continue to act in the same way during its mission performance. However, we feel the risks of irradiating flight hardware outweigh the advantages.

X. SUMMARY

We have discussed test and programmatic philosophies for COTS PCBs and radiation effects. These include discussions of:

- The many challenges with the testing of COTS PCBs'
- The role of mission hazard and duration on determining PCB usage and radiation test planning,
- The understanding of the criticality of the system in its mission profile,
 - The type of COTS PCB usage/radiation testing presented herein is best suited for non-critical applications with radiation testing required on the critical boards within that system,

We have provided new insights into test methodologies for COTS PCBs as well as examples of ground irradiation test results. It is the opinion of the authors that COTS PCB radiation testing does not substitute for full piecepart radiation hardness assurance (RHA) nor adequately quantify mission risk.

XI. REFERENCES

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